Marked up version showing changes made:

Abstract

An integrated circuit wafer element and an improved method for bonding the same to produce a stacked integrated circuit. An integrated circuit wafer according to the present invention includes a substrate having first and second surfaces constructed from a wafer material, the first surface having a circuit layer that includes integrated circuit elements constructed thereon. A plurality of vias extend from the first surface through the circuit layer and terminate in the substrate at a first distance from the first surface. The vias include a stop layer located in the bottom of each via constructed from a stop material that is more resistant to chemical/mechanical polishing (CMP) than the wafer material. The vias may be filled with an electrically conducting material to provide vertical connections between the various circuit layers in a stacked integrated circuit. [In this case, the electrical conducting vias are also connected to various circuit elements by metallic conductors disposed in a dielectric layer that covers the circuit layer. A plurality of bonding pads are provided on one surface of the integrated circuit wafer. These pads may be part of the vias. These pads preferably extend above the surface of the integrated circuit wafer. A stacked integrated circuit according to the present invention is constructed by bonding two integrated circuit wafers together utilizing the bonding pads. One of the integrated circuit wafers is then thinned to a predetermined thickness determined by the depth of the vias by chemical/mechanical polishing (CMP) of the surface of that integrated circuit wafer that is not bonded to the other integrated circuit wafer, the stop layer in the vias preventing the CMP from removing wafer material that is within the first distance from the first surface of the substrate of the wafer being thinned.]

1(Amended). An integrated circuit wafer comprising:

[a wafer comprising] a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

a plurality of vias extending a first distance from said first surface of said substrate into

said substrate, [from said first surface] said first distance being less than the distance between said first and second surfaces of said substrate, said vias having a bottom surface comprising a stop layer covering said bottom surface, said stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material.

7(Amended). [The integrated circuit wafer of Claim 1 further comprising:] An integrated circuit wafer comprising:

a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said vias comprising a stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material;

a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit layer; and

a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements.

REMARKS

The Examiner objected to Claim 1 because of the term "wafer comprising" is written twice. The above amendments to Claim 1 cure this defect.

The Examiner objected to the abstract as being too long. The above amendments to the abstract cure this defect.

The Examiner rejected Claims 1-10 under 35 U.S.C. 112, first paragraph. The Examiner maintains that the depth of the vias into the substrate is critical and that this feature is not enabled in the specification. Applicant traverses this rejection.

First, Applicant must point out that the specification teaches that the variation in depth is critical not the actual depth. The specification teaches that the depth of the vias determines the thickness of the wafer after thinning and that this variation in thickness must be a fraction of a micron (See the first full paragraph on page 2 and the discussion regarding Figures 2-9 on pages 6 through 9). The examples given in the specification teach specific exemplary depth ranges for the vias.

Second, etching a via in a silicon substrate to a precise depth within the stated range is known to the art. It is the inclusion of the stop layer in the bottom of the via that allows the variation in wafer thickness after thinning to be held to the needed tolerance. That feature is claimed in Claim 1.

The Examiner rejected claims 1-3, 5 under 35 U.S.C. 102(b) as being anticipated by Clements (US 4,954,875). Applicant submits that Claim 1 and the claims dependent therefrom are not anticipated by Clements.

Clements teaches a wafer having a via passing through the wafer in which the side walls of the via have a layer of silicon nitride. The present invention as now claimed requires the vias

to extend partially through the substrate and to have a layer of stop material on the bottom surface of the substrate.

The Examiner rejected Claims 6-10 under 35 U.S.C. 103(a) as being unpatentable over Clements as applied to Claim 1 and further in view of Hsuan, *et al.* (US 6,288, 642). Applicant submits that these claims as now amended are not obvious in view of these references. Applicant repeats the arguments made above with respect to the missing elements in Clements.

First, Hsuan does not teach the elements of Claim 1 that are missing from Clements. "The mere fact that a reference could be modified to produce the patented invention would not make the modification obvious unless it is suggested by the prior art." (*Libbey-Owens-Ford v. BOC Group*, 4 USPQ 2d 1097, 1103). "When the PTO asserts that there is an explicit or implicit teaching or suggestion in the prior art, it must indicate where such a teaching or suggestion appears in the reference" (*In re* Rijckaert, 28 USPQ2d, 1955, 1957). Hence, Applicants respectfully submit that the Examiner has not made a *primia facia* case for obviousness with respect to Claim 1.

With respect to Claims 7-10, the Examiner has not pointed to any place in the art at which the limitations of these claims are taught, no less, a motivation for combining such teachings with the teachings of the cited references. Since the Examiner, not the Applicant, has the burden of making such a showing, Applicant submits that the Examiner has not made a *primia facia* case for obviousness with respect to these claims. The above amendments to Claim 7 place these claims in independent form.

I hereby certify that this paper (along with any others attached hereto) is being sent by FAX to 703-872-9318.

Respectfully Submitted,
Gupta, et al.

by

Calvin B. Ward
Registration No. 30,896
Date signed and mailed: 9/11/02

18 Crow Canyon Court, Suite 305
San Ramon, CA 94583
Telephone (925) 855-0413
Telefax (925) 855-9214